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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/389,393	09/03/1999	HISASHI OHTANI	07977/204002	5375

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EXAMINER

BAUMEISTER, BRADLEY W

ART UNIT	PAPER NUMBER
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2815

DATE MAILED: 05/29/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

# Office Action Summary

Application No.

09/389,393

Applicant(s)

Ohtani et al. *hw*

Examiner

B. William Baumeister

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

## Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136 (a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

## Status

- 1) ☒ Responsive to communication(s) filed on Mar 25, 2003.
- 2a) ☐ This action is FINAL. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11; 453 O.G. 213.

## Disposition of Claims

- 4) ☒ Claim(s) 1-3 and 44-84 is/are pending in the application.
- 4a) Of the above, claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-3 and 44-84 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claims \_\_\_\_\_ are subject to restriction and/or election requirement.

## Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on \_\_\_\_\_ is: a) ☐ approved b) ☐ disapproved by the Examiner.  
If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

## Priority under 35 U.S.C. §§ 119 and 120

- 13) ☐ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).  
a) ☐ All b) ☐ Some\* c) ☐ None of:  
1. ☐ Certified copies of the priority documents have been received.  
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.  
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).  
\*See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).  
a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

## Attachment(s)

- 1) ☐ Notice of References Cited (PTO-892) 4) ☐ Interview Summary (PTO-413) Paper No(s). \_\_\_\_\_
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948) 5) ☐ Notice of Informal Patent Application (PTO-152)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s). \_\_\_\_\_ 6) ☐ Other:

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## **DETAILED ACTION**

### ***Specification/Claim Objections***

1. The specification and claims 73-78 are objected to because of the following informalities: both the specification (e.g., page 12, lines 1-) and stated claims recite that the lower conductive layer 4 (which has the higher oxidation rate) is composed of Ta and that the upper conductive layer 5 (which has the lower oxidation rate) is composed of Al. However, various references already made of record teach that Al has a higher oxidation rate than does Ta: e.g., IBM Technical Disclosure Bulletin 9503441 teaches that AlOx and TaOx have growth ratios of 23 and 15, respectively (table on page 442), and JP 6-265936 teaches that when not formed so thin as to constitute a superlattice, Ta is normally more difficult to oxide than Al col. 5, line 24-).

a. Thus, the Examiner questions whether (1) the specification and claims inadvertently reversed the order of Ta and Al from what was intended; or alternatively (2) whether the recited order is, in fact, intended and correct, indicating that the specific, respective oxidation rates depend upon the particular acid in which the anodic oxidation takes place. Appropriate explanation and/or correction is required.

2. Claims 44, 46 and 48 are objected to because of the following informalities: each claim first recites, "a semiconductor film," but later recites "a gate insulating film formed over the semiconductor region [sic: film]. Appropriate correction is required.

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*Claim Rejections - 35 USC § 103*

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) a patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

4. Claims 1-3 and 44-84 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ha '530 in view of Ota JP '615.

a. Ha discloses a top-gate polycrystalline Si TFT (claims 3 and 79-84) with a T-shaped, two-layer gate electrode employed over SiO<sub>x</sub> gate insulating layer 33 (col. 5, lines 15-) (claims 2 and 67-72) for the purpose of reducing drain leakage current. The two-layer gate is composed of a lower oxidizable metal having sufficiently good conductivity characteristics, such as Al or Ta, and the upper gate metal is composed of a material such as "chrome" [sic: chromium] having an oxidation rate which is lower than that of the first metal, or more specifically, a second material that is not oxidizable. This structure is then covered by an SiO<sub>x</sub> insulating layer 37. The two gate metal layers are initially deposited so as to have the same lateral width and are subjected to an anodic oxidation process which causes the lower layer to form an anodic oxide (e.g., AlO<sub>x</sub>) on the sides of only the lower gate portion, thereby producing a T-shaped gate having a thinner lower metal region that is laterally surrounded by the insulating metal oxide.

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The TFT semiconductor active region or film includes source/drain regions 32b/c; channel 32d; an a pair of regions formed therebetween, each region, in turn, comprising a first, offset portion 32e and a second, LDD portion 32a. All of these semiconductor regions are composed of polycrystalline silicon (“the same material as the channel”). Restated, under the broadest reasonable interpretation, the term, “the same material as the channel” reads on a plurality of regions that are composed of Si, irrespective of the regions’ specific impurity dopant levels.

Alternatively, even if “the same material as the channel” must be interpreted so narrowly (or is later amended) as to require that these respective regions also have the same dopant concentration as well (i.e., that the pair of regions are not doped differently from the channel), the claims would still be obvious. Ha teaches that in order to prevent tunneling, either LDD regions or alternatively offset regions (having the same doping as the channel) may be employed (e.g., col. 1, lines 42-47; col. 2, lines 3-5). Ha also teaches that the use of LDD regions in that invention is only “preferable” (col. 5, lines 42-47), indicating that the use of LDD regions is not necessary and that other functionally equivalent means for preventing tunneling (such as undoped offsets) may be employed. Also, Applicant acknowledges in the background section of the present specification that the use of LDD and offset regions were functionally equivalents for preventing tunneling and were conventionally known.

b. While Ha teaches that the upper metal layer has a lower oxidation rate for the purpose of producing a T-shaped gate, it does not disclose that the upper metal layer may also be composed of a material wherein its lower oxidation rate is greater than zero. But Ha further

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teaches that the use of chromium presents the problem of erosion during oxidation, and therefore Ha states that it is preferable to further include an additional, patterned protective insulating layer over the chromium layer to protect it during the oxidation process.

c. Ota teaches two-level metal gates that are both oxidizable, and which are, in fact, oxidized, thereby forming an inverted T-shaped gate for a bottom-type TFT. Specifically, Al gate layer 12 having the side portions 18 anodized to form AlOx; a Ta layer 14, most of which has been oxidized to form TaOx layer 20 (please note the Abstract and paragraph [0018] which recite that most--not all--of the Ta is oxidized); SiN insulating film 22; and Si film 24. Further, Ota teaches that the upper Ta layer is first etched to have a lateral width that is less than that of the of lower Al layer, but that upon oxidation some of the Ta--even though originally smaller in the lateral direction--still remains. Thus, this passage may be deemed to implicitly teach that Ta has a lower oxidation rate than that of Al. Ota also teaches that while chromium can be used for TFT gate electrodes, its use has the drawback that chromium has a high electrical resistance [0004]. Ota further teaches that the use of AlOx and TaOx provides better insulation than conventional SiN alone, and prevents pinholes present in the SiN from causing current leaks between the gate and adjacent conductive layers [0005] and [0019].

d. It would have been obvious to one of ordinary skill in the art at the time of the invention to have substituted within the Ha device an upper metal layer that is less oxidizable than the lower layer (as taught by Ha) but is still oxidizable to some extent for the purposes of (1) providing a T-shaped gate that reduces current leakage (as taught by Ha) while simultaneously

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providing a gate electrode that (1) has better insulation properties to prevent pinhole induced leakage between the gate and an adjacent conductive layer as taught by Ota (e.g., between the gate top and upper wiring layers for top-gate TFTs) and/or (2) obviates the need for the additional manufacturing steps required for providing an aligned insulator above the upper-gate layer as required by Ha, by instead using the resultant oxide of the upper conductive layer as the insulator (claims 49-54).

e. Regarding claims 55-60, it would have been obvious to one of ordinary skill in the art at the time of the invention to use at least two of the materials from the recited Markush group (Ta and Al) because Ha teaches that either Al or Ta may be employed for anodic oxidized TFT gates.

f. Regarding claims 73-78, assuming that the recitation of Al and Ta was inadvertently reversed for the reasons set forth above, it would have further been obvious to specifically employ Ta for the upper, less oxidizable gate layer and Al for the lower, more oxidizable layer because Ha teaches that either Al or Ta may be employed for TFT gates, and Ota and other various references previously cited and made of record teach that Ta has a lower oxidation rate than that of Al.

i. Alternatively, assuming the claims' recited order for Al and Ta is correct, it nonetheless would have been obvious to have formed the layers of these particular materials because Ha teaches that either Al or Ta may be employed for anodizable TFT gates. Further, since Applicant has not expressly disclosed any details regarding the method by which the two

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materials are oxidized to achieve the T-shaped structure (e.g., such as the particular oxidizing acid employed), but only discusses them indirectly through the reference of other Japanese patent documents, Applicant is effectively acknowledging that the particular method for simultaneously oxidizing Al and Ta--such that the Ta will be more greatly oxidized--is conventional.

g. Claims 45-48 variously further set forth that the distance between the first portion and the source or drain region (i.e., the width of the second portion, corresponding to region 32a of Ha when Ha is combined with Ota in the manner described above) is either larger (claims 45 and 46) or alternatively equal to or less than (claims 47 and 48) a thickness of the first (lower) conductive layer.

i. As an initial matter, the Examiner notes that a structure formed according to Ha/Ota would necessarily have to satisfy one of these two complementary relationships (either "greater than" or alternatively, "equal to or less than"), and as such, one of the two complementary limitations set forth by these two claim sets would inherently have to be met. Furthermore, it would have been obvious to set this ratio specifically to satisfy either set of conditions for the following reasons.

ii. Ha discloses that the lower conductor has a thickness of about 2500 angstroms (col. 5, lines 19-21). Ha also discloses that the width of anodic oxide layers 36a/b may have a width anywhere within the range of 1000 to 10,000 angstroms (col. 5, lines 60-62). Furthermore, the upper conductor formed according to Ha/Ota would necessarily have a lateral width that is greater than that of the resultant lower conductor and would necessarily have a

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width that extends laterally a distance less than that of the lower anodic oxide since both conductive layers are originally formed to have the same lateral dimensions and the upper conductor has a lower oxidation rate than does the lower conductor. As such, when the anodic oxide 36a/b is set to the disclosed lower width limit of 1000 angstroms (claims 47 and 48), the upper conductor would necessarily extend some less distance resulting in a first portion width "x" that is necessarily less than 1000 angstroms and therefore necessarily less than the lower conductor's 2500 angstrom thickness.

iii. At the other, upper limit disclosed by Ha wherein the anodic oxide 36a/b is set to the width of 10,000 angstroms (claims 45 and 46), the width of the first portion "x" would necessarily be greater than 2500 angstroms if the second conductive layer's anodic oxide growth rate is at least 1/4 of that of the first conductive layer's anodic oxide growth rate ( $1/4 * 10,000\text{-angstrom width} = 2500\text{-angstrom thickness}$ ). As this would be the case for the various oxidizable materials that are typically employed TFT gates, the condition would necessarily result. (Note for example, IBM Technical Bulletin 9503441, which teaches that the anodic oxidation growth rates of TaOx and AlOx are 15 angstroms/volt and 23 angstroms/volt, respectively (table on page 442), resulting in a growth rate ratio of 0.65, which is significantly greater than 0.25.)

h. Regarding claims 61-66, when an oxidizable second conductor is formed on top of the lower conductive layer as taught by Ota for the reasons set forth above, the resultant value of "x" (the distance between the upper gate layer edge and the edge of the lower anodic oxide) is a function of (1) the initial width to which the gate's two conductive layers were set prior to the

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oxidation step, and (2) the differential oxidation rate of the two specific conductive materials employed. Further, as was stated above, Ha teaches that (lower) anodic oxide layer 36a/b may have a width of as low as 1000 angstroms. This 1000-angstrom lower-anodic-oxide-width precondition results in "x" necessarily being less than 1000 angstroms because the upper conductive layer has a lower oxidation rate. While specific initial-width and oxidation-ratio parameters could possibly be selected that would result in "x" being less than the alternative claimed lower limit of 500 angstroms, it would have been obvious to one of ordinary skill in the art at the time of the invention to have selected the cited parameters so as to produce an "x" that is greater than 500 angstroms because at "x" widths below this value, the probability would significantly increase that quantum tunneling between the upper gate conductor and adjacent conductive layers would occur; thus it would have been obvious to maintain "x" above this 500-angstrom level so as to enable the TFT to operate as intended without the need for providing additional insulating layers adjacent the upper gate oxide to inhibit parasitic quantum tunneling.

5. Claims 1 and 44-84 are alternatively rejected under 35 U.S.C. 103(a) as being unpatentable over Ha/Ota as applied to the claims above and further in view of Yamazaki '998 (previously made of record in paper #3). Ha/Ota teaches or renders obvious all of the elements of the claims, as explained above.

a. Even assuming *arguendo* that insufficient motivation has been proffered for combining these references to produce the resultant invention, Yamazaki teaches TFTs having

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anodized gate electrodes, albeit not T-shaped, two-layer gates. It would have been obvious to one of ordinary skill in the art at the time of the invention to have combined either of Ha/Ota in the manner set forth above so as to provide a T-shaped gate having anodic oxidized top and side surfaces for the purpose of providing a gate insulator with high resistivity (e.g., col. 5, lines 1-) and more uniform oxide coverage than that afforded by other conventional insulators (e.g., col. 3, lines 1-18).

b. In further regard to the newly added limitations relating to the width of the upper anodic oxide and the width/thickness relationship claimed, Yamazaki provides further evidence (1) that it was known by those of ordinary skill in the art at the time of the invention how adjusting the thicknesses of anodic gate oxide sidewalls can effect TFT manufacturing (such as in realizing channel offsets) and performance (such as in influencing carrier tunneling and leakage); and (2) therefore, that these claimed range and relationship do not produce any unexpected results.

### ***Response to Arguments***

6. Applicant's arguments with respect to the claims have been considered but are either moot in view of the new ground(s) of rejection or are not persuasive for the reasons set forth hereinabove.

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**INFORMATION ON HOW TO CONTACT THE USPTO**

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to the examiner, **B. William Baumeister**, at **(703) 306-9165**. The examiner can normally be reached Monday through Friday, 8:30 a.m. to 5:00 p.m. If the Examiner is not available, the Examiner's supervisor, Mr. Eddie Lee, can be reached at (703) 308-1690. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (703) 308-0956.

A handwritten signature in black ink, appearing to read "B. William Baumeister". The signature is stylized with a large, looping initial "B" and a long, sweeping horizontal stroke across the middle.

B. William Baumeister

Patent Examiner, Art Unit 2815

May 24, 2003